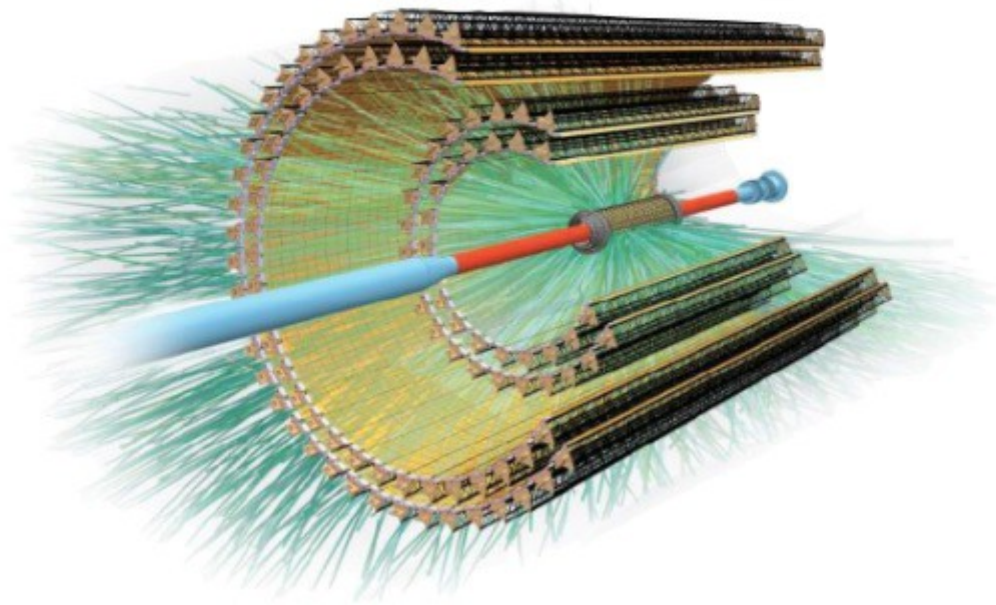


# Characterization of the Outer Barrel modules for the upgrade of the ALICE Inner Tracking System



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# Outline

- ITS Design Objectives
- ITS design elements overview
- Modules test-stand for electrical characterization
- Some prototypes results

# ITS Upgrade Design Objectives

Improve impact parameter resolution by a factor  $\sim 3$  in  $r$  and  $\phi$

$\sim 5$  in  $z$  at  $p_T = 500 \text{ MeV}/c$

- get closer to IP: 39mm  $\rightarrow$  22mm (innermost layer)
- reduce material budget:  $\sim 1.14\% X_0 \rightarrow$   
 $\sim 0.3\% X_0$  (inner layers)  
 $\sim 1.0\% X_0$  (middle and outer layers)
- reduce pixel size:  $50 \times 425 \mu\text{m} \rightarrow 30 \times 30 \mu\text{m}^2$

Improve tracking efficiency and  $p_T$  resolution at low  $p_T$ :

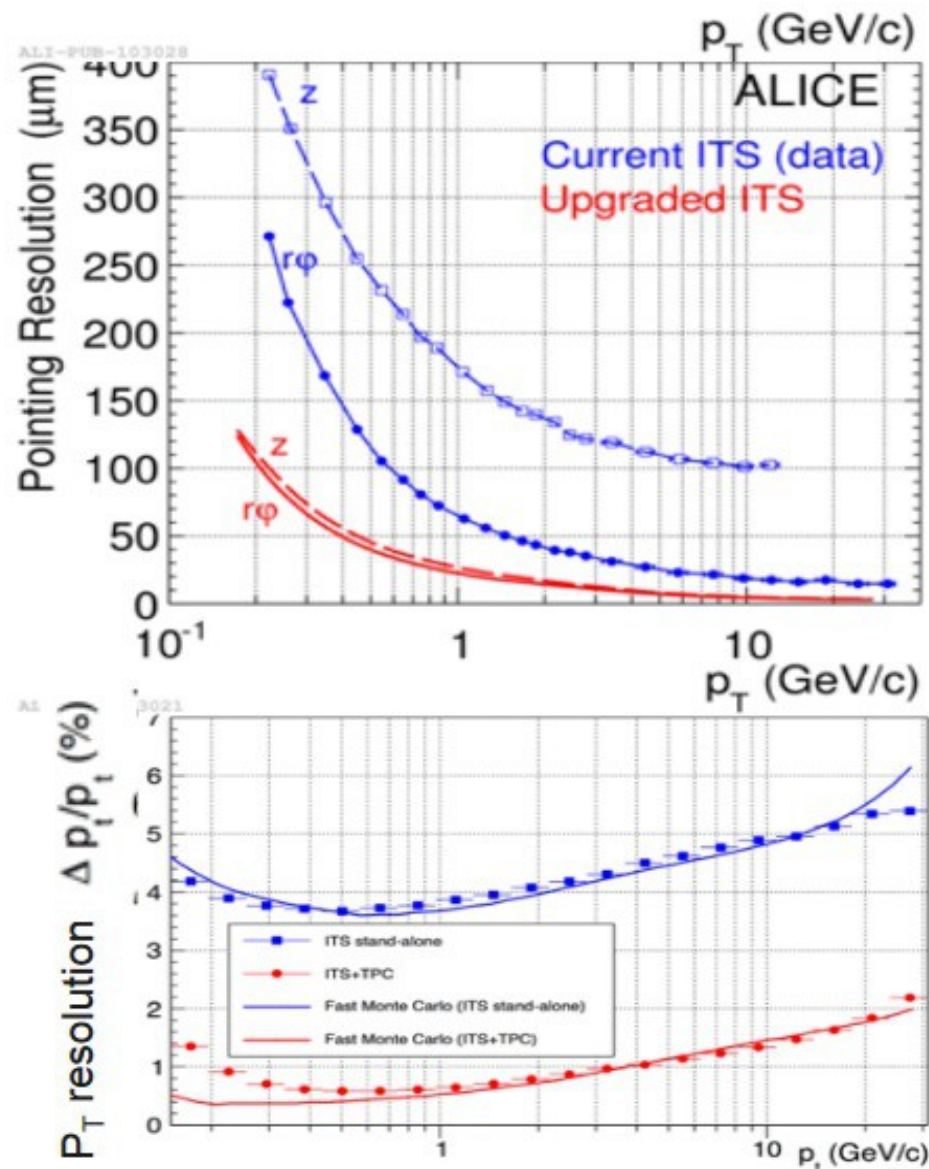
- increase granularity: 6 layers  $\rightarrow$  7 pixel layers

Improve readout rate:

- increase readout rate of Pb-Pb from present 1kHz up to 100 kHz and 400kHz for pp

Fast insertion and removal:

- possibility to replace non-functioning detector modules during yearly shutdown



# ITS Upgrade requirements

## Pixel Chip Requirements

Parameter	Inner Barrel	Outer Barrel	ALPIDE
Silicon thickness	50 $\mu$ m	100 $\mu$ m	✓
Spatial resolution	5 $\mu$ m	10 $\mu$ m	~ 5 $\mu$ m
Chip dimension	15mm x 30mm		✓
Power density	< 300mW/cm <sup>2</sup>	< 100mW/cm <sup>2</sup>	< 40mW/cm <sup>2</sup>
Event-time resolution	< 30 $\mu$ s		~ 2 $\mu$ s
Detection efficiency	> 99%		✓
Fake-hit rate *	< 10 <sup>-6</sup> /event/pixel		<<< 10 <sup>-6</sup> /event/pixel
NIEL radiation tolerance **	1.7x10 <sup>13</sup> 1MeV n <sub>eq</sub> /cm <sup>2</sup>	10 <sup>12</sup> 1MeV n <sub>eq</sub> /cm <sup>2</sup>	✓
TID radiation tolerance **	2.7Mrad	100krad	tested at 350krad

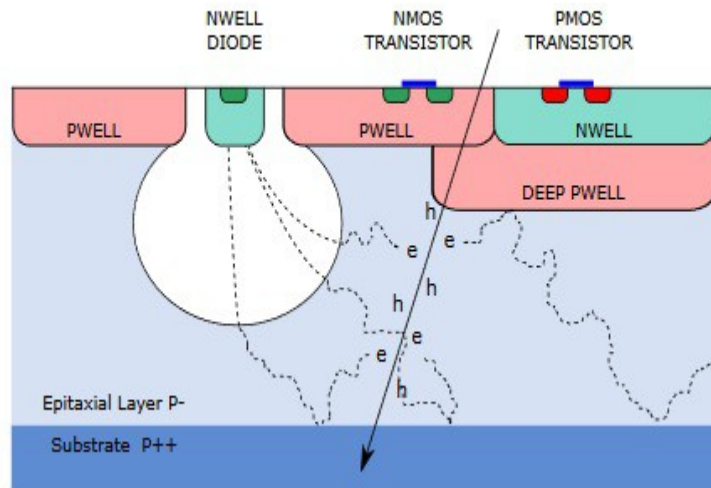
## ITS Coverage Requirements

$\eta$  coverage:  $|\eta| \leq 1.22$   
 $r$  coverage: 22 – 400 mm  
 $z$  coverage: Inner Layers L = 290 mm  
Middle Layers L = 900 mm  
Outer Layers L = 1500 mm

## MAPS Pixel ( $30 \times 30 \mu\text{m}^2$ )

## Building blocks

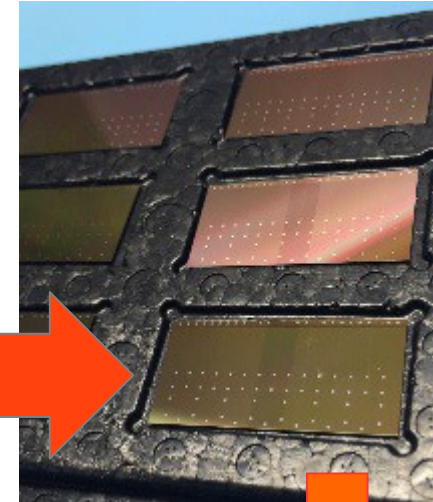
CMOS Pixel Sensor using TowerJazz 0.18 $\mu\text{m}$  CMOS Imaging Process



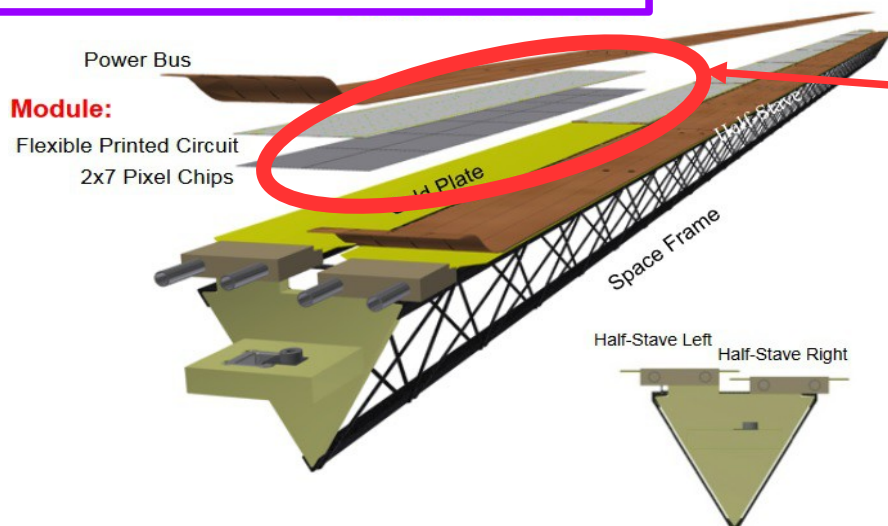
### Tower Jazz 0.18 $\mu\text{m}$ CMOS

- feature size 180 nm
- metal layers 6
- Suited for high-density, low-power
- Gate oxide 3nm
- Circuit rad-tolerant

**ALPIDE Chip:**  
1024x512 pixels ( $30 \times 15 \text{ mm}^2$ )



**OB staves: 7+7 modules**  
**MB staves: 4+4 modules**



**OB/MB Module 7+7 chips**

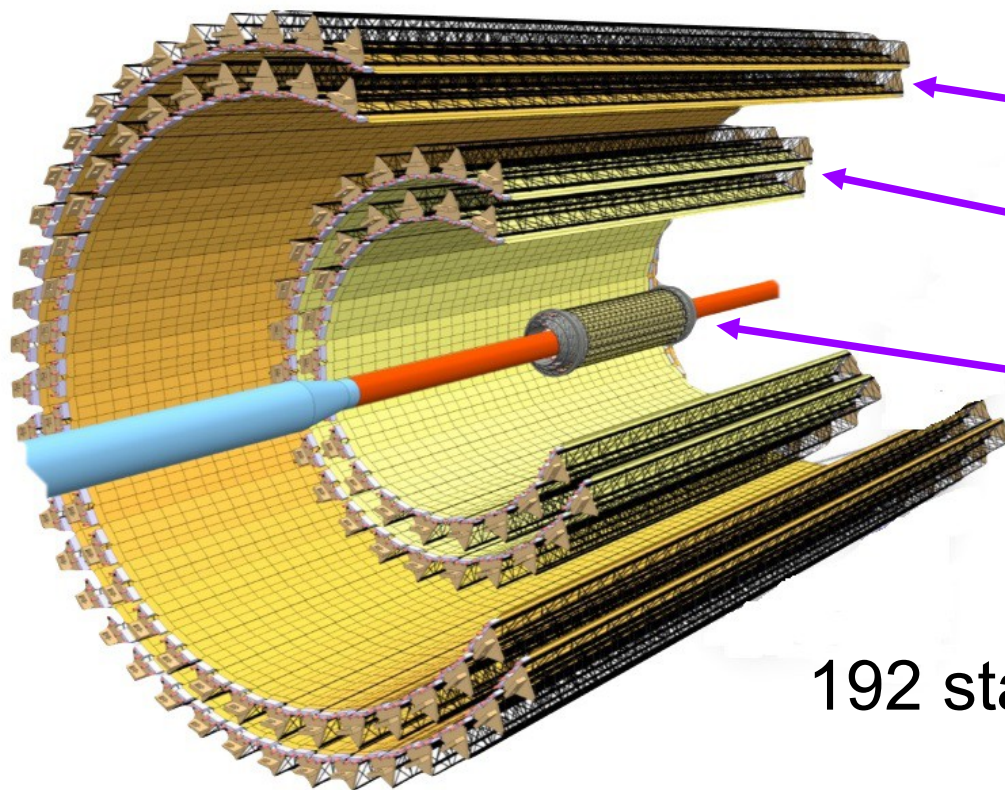


cross cables  
(connection to power bus)

single chip

## ITS Upgrade Overview:

12.5 Gigapixels  
~ 10 m<sup>2</sup> active surface



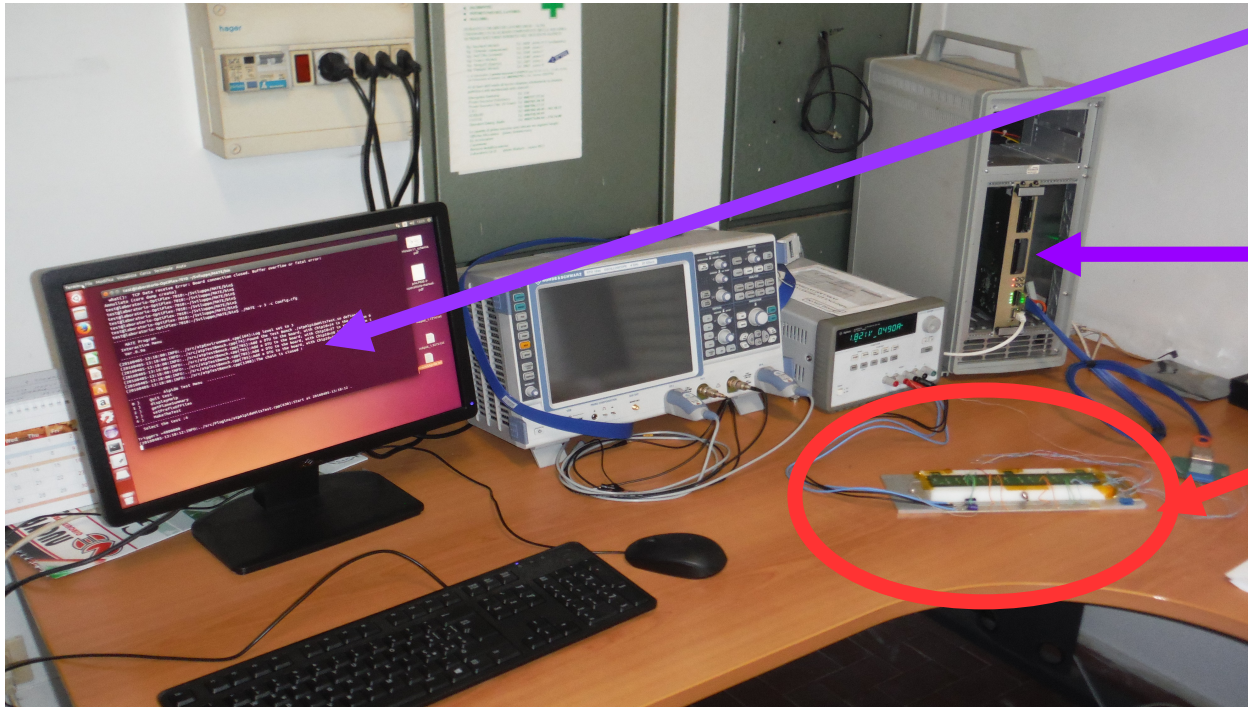
### 7 layers:

- 2 Outer Layers
- 2 Middle Layers
- 3 Inner Layers

192 staves: 90 (OL) 54 (ML), 48 (IL)

Layer #	6	5	4	3	2	1	0
n. of Chip	9408	8232	3360	2688	180	144	108
n. of Modules	672	588	240	192	20	16	12
n. of Staves	48	42	30	24	20	16	12

# Module test set-up



Test software  
(MATE package)

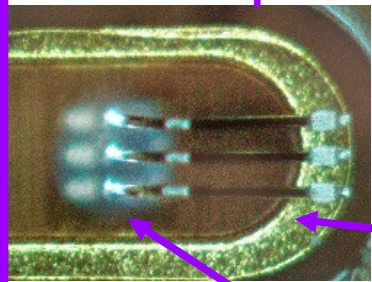
Communication Board  
(MOSAIC Board)

Module under test  
(FPC side)

Data cables

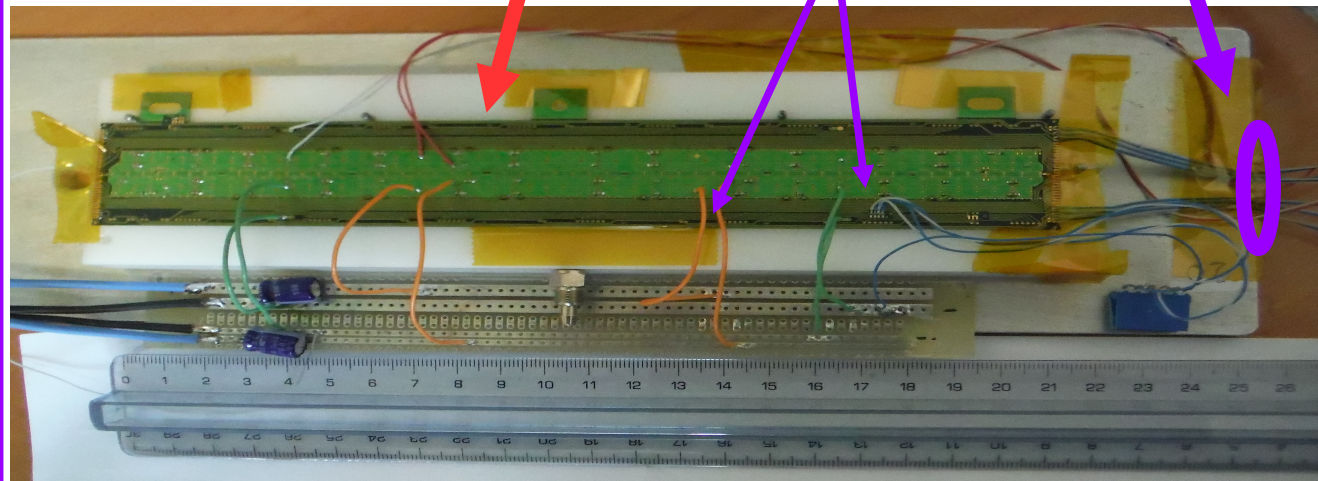
Power Cables

## FPC - Chip wire bonding detail



Flexible  
Printed  
Circuit

Glue  
Chip Pads



# Outer Barrel modules Status

## OB Modules Prototypes

So far a series of OB modules prototypes was built using pALPIDE Version 3 chips: 6 modules and 1 OB stave (with 2 modules)

These prototypes were used to define the building modules and stave procedure.

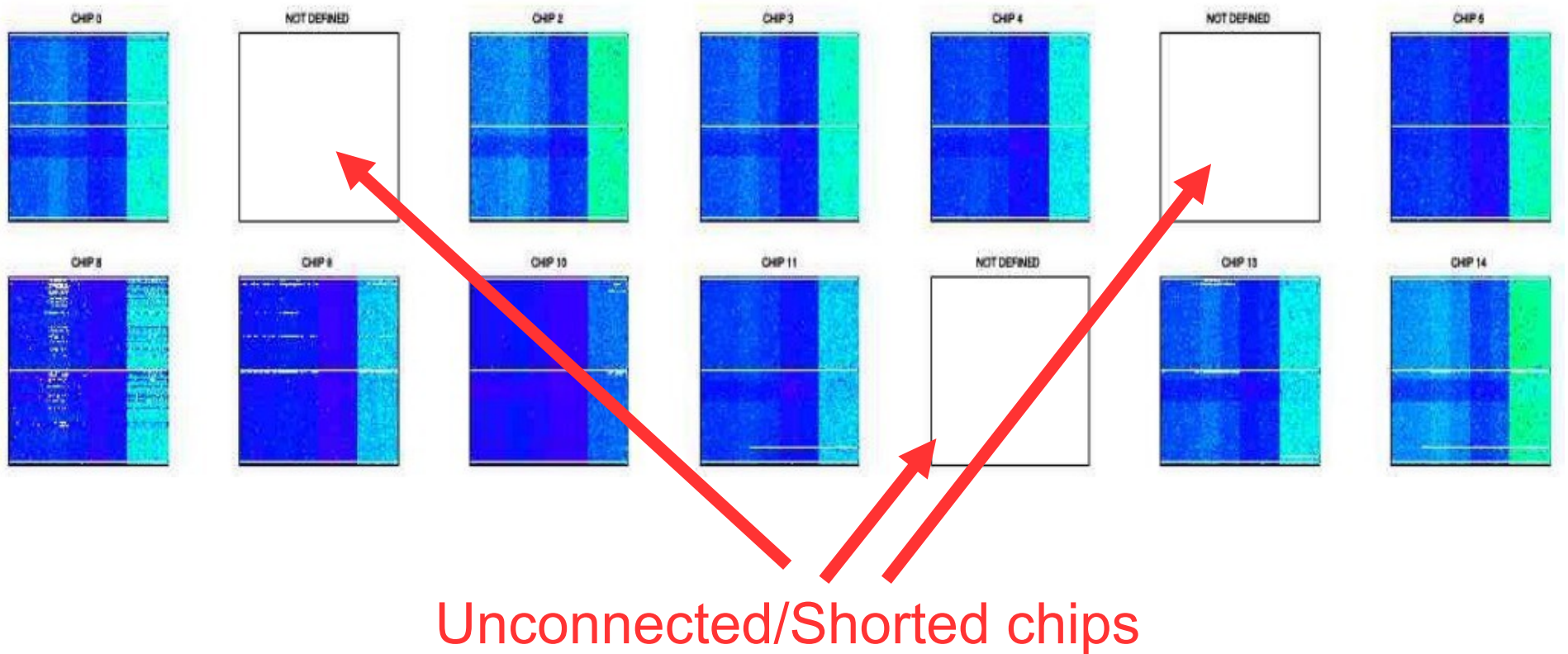
The pALPIDE chip contains a self-injection charge feature that allow to test the read-out chain of every single pixel. This feature, handled by the MATE framework, is used

- to check the inter-modules interconnections (wire bonding integrity)
- to map dead pixels
- to perform the full module readout rates characterization

## Next steps:

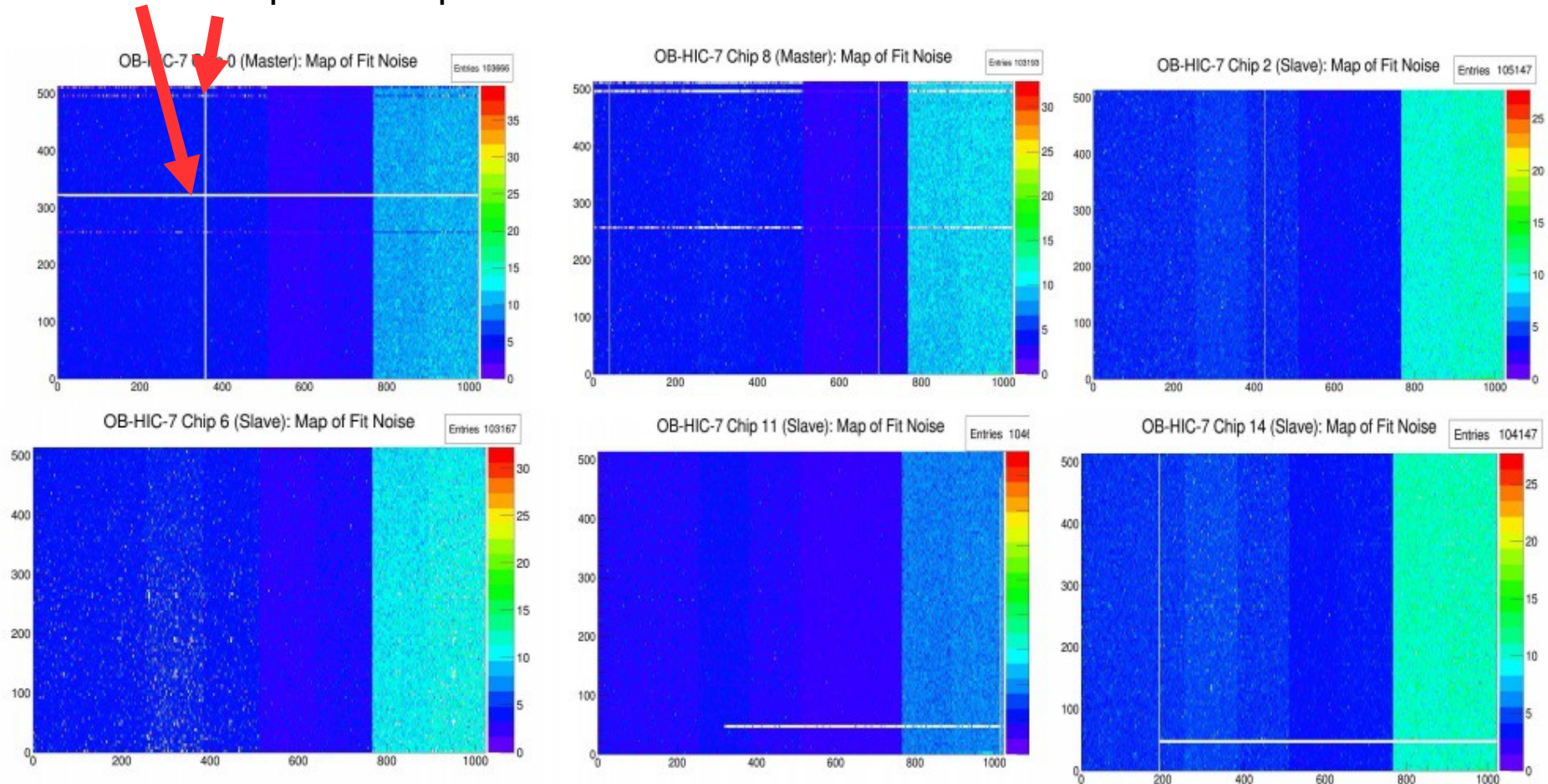
Pre-series production is starting (~20 units) with final ALPIDE chips in Oct – Dec 2016

## Some prototype results: global module status



## Some prototype results: single chip details

Broken lines/ bad pixels map



With this setup in ~30 minutes is possible to perform the full module electrical characterization and the full map of bad pixels.

# Conclusions

The ALICE ITS upgrade program require the mass production of ~ 1700 Outer Barrel modules.

A procedure was defined in order to perform a fast functional characterization of the produced modules.

This procedure will be implemented in the production of the next final version of the modules.

## References

### **ALICE ITS upgrade TDR**

<https://cds.cern.ch/record/1625842?ln=en>

### **The upgrade of the ALICE ITS**

by Stefania Beole,

VERTEX 2016 Conference

[https://indico.cern.ch/event/452781/contributions/2297487/attachments/1343570/2024447/VERTEX2016\\_beole.pdf](https://indico.cern.ch/event/452781/contributions/2297487/attachments/1343570/2024447/VERTEX2016_beole.pdf)

### **MOSAIC Board description**

by Giuseppe De Robertis,

MPGD 2015 Conference, Trieste 12-15 October 2015

<https://agenda.infn.it/contributionDisplay.py?contribId=86&sessionId=8&confId=8839>